



A CLOCK GATED COLPITTS CMOS QUADRATURE VCO FOR LOW POWER APPLICATIONS

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ABSTRACT

The need for extra elements for coupling will add noise and increase power dissipation to the LC-QVCOs. To improve the phase noise, various experiments are done to modify the coupling networks. A new clock gated quadrature voltage-controlled oscillator (QVCO) using differential Colpitts oscillator is presented. The coupling technique presented is applicable to N differential Colpitts QVCOs for multiphase signals generation and a clock gated multiphase QVCO is presented. The main advantage of this technique is that, here we are not using any coupling networks. The clock gated QVCO is combined of two similar current-switching differential Colpitts VCOs in which the first core VCO is connected to the second in an in-phase manner, and the second core VCO is connected to the first in an anti-phase manner. For this connection the substrates of the interconnected transistors as well as the substrates of MOS varactors are used. A linear (sinusoidal) analysis is showed that verify that the VCO circuit generates quadrature waveforms.

Keywords – quadrature oscillator, low-phase noise, multiphase, Current-switching Colpitts-oscillator.

I. INTRODUCTION

Quadrature and multiphase voltage-controlled oscillators are essential basic blocks in almost all the present transceiver front-ends, whose functioning can notably influence the functioning of the entire communication system. Several methods for quadrature signal generation are existing. Injection locked LC quadrature voltage-controlled oscillators based on first-harmonics and super-harmonics. Injection has become commonly accepted method in RF circuits since their phase noise is favourable.

LC-QVCOs have two major blocks; a couple of same LC-VCOs and combination circuit, here the two blocks will affect the entire communication system output. To progress the phase noise in formerly discussed LC-QVCOs, we are mainly concentrating on the combination circuit, experimenting a variety of active or passive, combination networks, as the central VCO will be approximately in the interconnected style.

In usual interconnected LC-VCOs, the noise formed by the active elements disturbs the VCO outputs at their zero crossings, i.e., the highest noise sensitivity point. On the other hand, in Colpitts

oscillators, the highest noise level, i.e., the highest of the impulse sensitivity function, formed by the central transistors is united with the smallest oscillator sensitivity points. Therefore, as shown, Colpitts oscillators have better cyclostationary noise values and possibly, an improved phase noise values when evaluating with the usual interconnected LC-VCOs. In formerly discussed QVCOs, differential Colpitts oscillators have been changed with the interconnected oscillators, thus obtaining a smaller phase noise. In two matching Colpitts VCOs are combined to each other via four parallel connecting transistors. But the parallel transistors will waste power and also disgrace the phase noise of the QVCO. To decrease the cause of noise of the connecting transistors, an arrangement known as noise-degenerated has been proposed while the connecting transistors are put in sequence with central transistors. So the phase noise and power usage can be decreased, stacking of transistors reduce the voltage headroom. In the QVCO discussed in and passive elements can be used in place of active coupling elements.

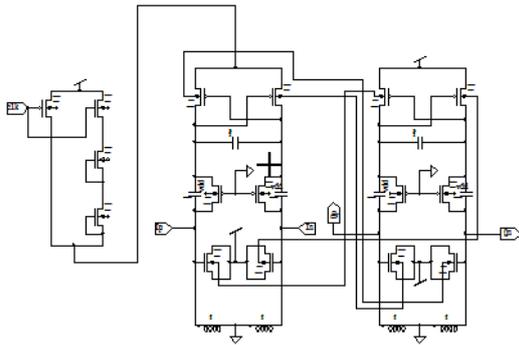


Fig.1. Schematic of the proposed clock gated QVCO

Here in mostly discussed Colpitts QVCOs additional circuits are used for connecting, which will reduce the whole functioning and efficiency of the QVCO and the chip area get increased. Also, if any irregularities between connecting devices occurs, it will lead to the balancing of the entire circuitry and shows phase error. This work presents an enhanced low-phase noise low-power clock gated quadrature voltage-controlled oscillator in which two similar differential Colpitts VCOs are connected without extra connecting devices which will reduced the phase noise and power usage.

Fig .2 Coupling is done by gate-bulk and bulk-drain capacitances

The proposed clock gated quadrature VCO and its analysis are added in the next section. Simulation values and an evaluation of its working with formerly discussed quadrature VCOs are showed in Section III. Conclusions are drawn in Section IV.

II. ANALYSIS OF THE PROPOSED CLOCK GATED QVCO

The proposed clock gated quadrature VCO is shown in Fig 1. The circuitry is made of two similar differential Colpitts VCOs which are connected in an “in-phase anti-phase” manner. As shown in Fig. 1, no extra connecting devices are used, also a power saving circuitry is used which will reduce power usage and delay.

As shown in Fig.1 the bulks of the switching transistors (nodes a and b of $M_{sw,1,2}$) of the first VCO are connected to the bulks of the MOS varactors (nodes a and b of $M_{var,3,4}$) of the second VCO in an “anti-phase” scheme, and the bulks of the switching transistors(nodes c and d of $M_{sw,3,4}$) of the second VCO are connected in an “in-phase” scheme to the bulks of the MOS varactors (nodes c and d of $M_{var,1,2}$) of the first VCO. Since in a technology with P-type wafer the PMOSFETs are placed in separate wells, their bulks can be connected to different potentials. Thus, by selecting the switching transistors and MOS varactors as P-type, there is no need for the use of the triple-well technology option.

In this circuit, the substrates of the MOSFETs are not in a floating state. The substrate potential is set

by the network combination of V_{dd} , source-substrate diodes in M_{sw} , the substrate- source/drain diodes in M_{var} and V_{tune} . The layout techniques such as Guard ring can be used for the purpose of reducing the effects of substrate noise on the phase noise. The potential at nodes a, b, c and d of the circuit can be fixed at any desired value by connecting them to a desired potential via four resistors.

The main idea in the proposed clock gated QVCO is to use the intrinsic capacitances of the core VCO’s transistors instead of some additional connecting devices. As shown in Fig. 2, the gate-bulk and the bulk-drain capacitances of the switching transistors, and the gate-bulk capacitances of the MOS varactors play the role of connecting devices and provide the injection path for coupling signals, thus avoiding the require for any additional AC coupling capacitors and DC biasing resistors. To reduce the noise involvement of the core VCOs to the whole phase noise, the noise-wise better Colpitts structure replaces the usual interconnected LC-VCOs. To show that a 90 phase difference present between the outputs of the proposed clock gated circuit, i.e., I+, I- and Q+, Q- in Fig. 1 are in quadrature, a linear analysis is presented as follows. In this analysis it is assumed that the waveforms are sinusoidal.

Table .1 parameter values for Simulations of QVCO

Due to the symmetry of the proposed clock gated circuit in Fig.1 the amplitude of all output voltages (i.e. I+, I- and Q+,Q-) are equal. Because of the differential arrangement of the core VCOs, there is a 180 phase shift between the potentials of the nodes I+ and I- and also between those of Q+ and Q-. Applying KCL at nodes and, following can be written (nodes and are virtual ground in Figs. 3.1 and 3.2): where V_a and V_b are the phasors of the voltages at nodes a and d, and C_{gb} , C_{bs} and C_{bd} are the intrinsic gate-bulk, bulk-source and bulk drain capacitances of the transistors respectively.

Since the transistors act as common-gate amplifiers, the voltage of the drain of this transistors (i.e. I+,I- and Q+,Q-) are amplified versions of their source potentials (i.e. $x+$, $x-$ and $y+$, $y-$).

Parameter	Value	Parameter	Value
$(W/L)_{M_{sw}}$	38 $\mu\text{m}/0.18 \mu\text{m}$	C_1	1 pF
$(W/L)_{M_{1-4}}$	22 $\mu\text{m}/0.18 \mu\text{m}$	C_2	0.5 pF
$(W/L)_{M_{var}}$	300 $\mu\text{m}/0.18 \mu\text{m}$	V_{dd}	1.8 volt
L	1 nH	V_{tune}	0.85 volt
r_L	1 Ω		

Due to the symmetry of the circuit, the amplitude of the voltages at nodes, a, b, c and d are the same, i.e., $V_a=V_d$. Therefore the absolute values of the left-hand side and the absolute values of their right-hand side are equal, as expressed in at the bottom of the page. At this point it is worth mentioning that, while occurrence of both possible

order of phases, i.e., potential at I+ leading or lagging that of q+, have been reported in literatures and also shows the same thing, numerous simulations performed in this work always showed a unique order of phases, i.e., potential at Q+ always led that of I+. Another thing to be noted is although the above study was based on sinusoidal waveforms, simulations showed that even for non-sinusoidal waveforms which will result from the low quality factor of the tank circuit, the proposed QVCO still does produce vigorous quadrature outputs.

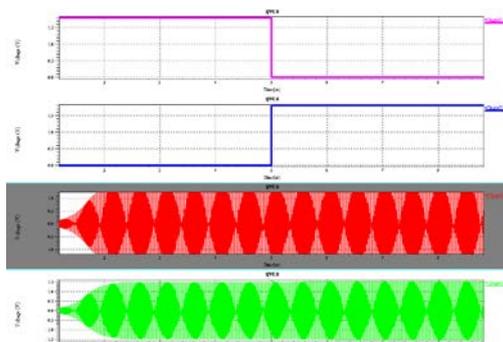
In this circuit, coupling factor K is defined as the ratio of coupling current to switching current i.e. $K_c = I_{cp}/I_{cw}$, for circuit parameters in Table I. While in a small signal region the term is almost constant for a particular technology, the desired coupling factor can be realized by changing the voltage gain, i.e., changing the size of M1-4 and ratio of C1 and C2.

III. SIMULATION RESULTS

The proposed clock gated quadrature Colpitts VCO is designed and simulated in a standard 0.18- m RF-CMOS technology. The performances of different QVCOs are evaluated. Fig. 3 shows the simulated output waveforms using the circuit parameter values shown in Table I. The ohmic loss of each inductor was defined as a series resistor rL with 1 ohm per each nH of inductance. Since no extra elements were used for coupling, no parasitic element is imposed on the tank circuit results the tuning ranges wider.

Fig.3 output waveform of clock gated QVCO

According to calculations, oscillation frequency varies from 4.95 to 5.92 GHz when is swept from 0 to 1.8 V, results in a tuning range of 18%, as shown in Fig. 4. The total dc current drawn from a 1.8-V power supply is 4.44mA leading to 8



mW total power consumption.

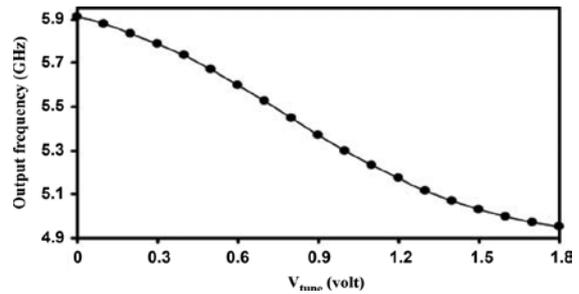
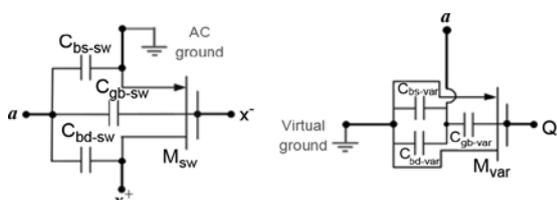


Fig. 4 Tuning range simulated frequency of proposed clock gated QVCO.

The simulated phase noise of the proposed clock gated QVCO at 5.4GHz centre frequency is compared to that of in Fig. 5. The parameters of each circuit are chosen such that both have the same oscillation frequency and power dissipation for the simulation.

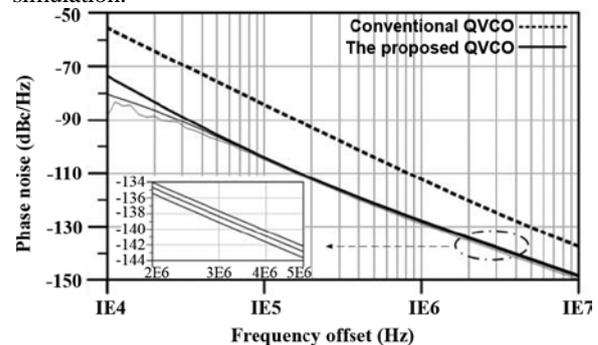


Fig.5 simulated phase noise of proposed clock gated QVCO

As we assumed, the phase noise in the proposed circuit is appreciably improved, which is due to the reduction of extra coupling networks and the clock gated method used. As Shown in Fig. 5, changing the coupling factor will results vary in the phase noise. However Monte Carlo analysis shows no deprivation of phase accurateness due to transform of coupling factor.

CLOCK GATED MULTIPHASE QVCO

We can make use of the same method for producing multiphase signal generation named clock gated multiphase QVCO. Here Coupling of similar LC-VCOs in a circuit such that N-1 the core VCOs are connected to each other in an “in-phase” manner, and the Nth core is connected to the first one in an “anti-phase” manner is a usually used technique for multiphase signals generation. Widening the same idea to the proposed design, as shown in Fig.3, the proposed coupling method can be practicable to numerous core Colpitts VCOs to produce multiphase signals. The proposed clock gated multiphase QVCOs can produce multiphase signals π/N with phase shifts (N=1, 2, 3..... is the number of core VCOs).

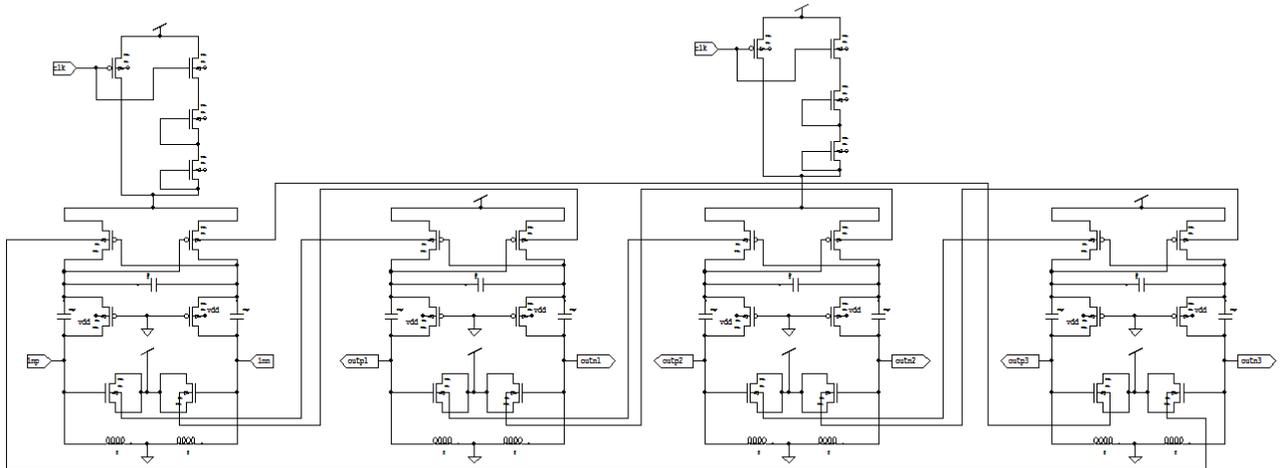


Fig.6 Schematic of the proposed four phase clock gated QVCO

As a usual case, a four-stage multiphase Colpitts VCO is implemented and simulated with circuit parameter values of Table 3.1 in a 0.18- μm RF-CMOS technology. The extracted simulation outputs show that the phase noise of the proposed clock gated four-phase QVCO is -139 dB/Hz at 3 MHz frequency offset from 5.25 GHz centre frequency, while drawing 10.5 mA from a 1.8-V power supply, giving an 191.1 dB.

IV. CONCLUSION

In this paper, usual LC-VCOs are substituted with the noise-wise better current-switching Colpitts VCOs. Injection-locked quadrature oscillators are usually combined of two separate parts: two core VCOs and some coupling devices, in which every element contribute to the phase noise performance. For better performance of the QVCO, we need to improve the phase noise by reducing the coupling network. Also to reduce the power dissipation due to the coupling circuitry, coupling devices were deducted by making use of the bulks of switching transistors and the bulks of the MOS varactors in the Colpitts core.

An analysis of the working of the clock gated proposed QVCO using a linearized model of the circuit is presented and shows matching with simulation results. The proposed design method can also be used to couple identical Colpitts VCOs for production of multiphase signals.

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